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10/698,610	10/31/2003	Marc Gandar	M2006-700010	9895

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EXAMINER	
TIV, BACKHEAN	

ART UNIT	PAPER NUMBER
2151	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/698,610	GANDAR, MARC	
	Examiner	Art Unit	
	BACKHEAN TIV	2151	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *RCE 7/9/08* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Detailed Action

Claims 1-9 are pending in this application. This is a response to the RCE filed on 7/9/08.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 1, recites, "each device of the plurality of devices comprising a communication circuit connected to a processing unit and **comprising a plurality of addresses, each address being associated with one of a transmission indicator or a reception indicator,** wherein each address is associated with a memory containing an information frame that can be at least one of modified and read by the processing unit and **wherein only a single device of the plurality of devices includes one of the plurality of addresses associated with the transmission indicator**", there is a conditional statement in this limitation. The "plurality of addresses, each address being associated with **one of** a transmission indicator **or** reception indicator". One ordinary skill in the art would interpret this limitation as, " plurality of addresses, each address being associated with reception indicator", if claim 1 were to be interpreted in this manner, then the limitation "wherein only a single device of the plurality of devices includes one of the plurality of addresses associated with the transmission indicator",

would be indefinite since each address is being associated with reception indicator and not the transmission indicator.

In another interpretation, " **each device of the plurality of devices** comprising a communication circuit connected to a processing unit and plurality of addresses, each address being associated with transmission indicator", claim 1 requires that each device have a plurality of addresses that are associated with a transmission indicator. Claim 1 further recites, " **wherein only a single device of the plurality of devices** includes one of the plurality of addresses associated with the transmission indicator". Claim 1 is unclear and indefinite taken this interpretation since, part of the claim requires that all of the device addresses is associated with a transmission indicator, and part of the claim requires, only one device includes a plurality of addresses associated with transmission indicator.

Claims 2-6 are rejected based on dependency of claim 1.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Publication 2002/0169886 issued to Saito et al.(Saito) in view of US Patent 5,666,363

issued to Osakabe et al.(Osakabe) in further view of US Patent 7,143,187 issued to Takeda et al.(Takeda).

As per claim 1, Saito teaches a method for exchanging information frames over a network between a plurality of devices, each device of the plurality of devices comprising a communication circuit connected to a processing unit (Fig.1. there is communication between the controller and devices), each address being associated with one of a transmission indicator or a reception indicator, wherein each address is associated with a memory containing an information frame that can be at least one of modified and read by the processing unit and wherein only a single device of the plurality of devices includes one of the plurality of addresses associated with the transmission indicator(Fig.3,8,para.0058), the steps of:
having a master device periodically transmit an address of the plurality of addresses(Fig.4,para.0017, 0063); and responsive to transmission of the address by the master device(para.0058-0060).

Saito however does not explicitly teach having the communication circuit of the device for which the address transmitted by the master device is associated the transmission indicator transmit the information frame contained in the memory associated with the address and provide its processing unit with an identifier of the address; and having the communication circuit of each device for which the address transmitted by the master device is associated with the reception indicator write into the

memory associated with the address of the information frame and provide its processing unit with an identifier of the address.

Osakabe teaches having the communication circuit of the device for which the address transmitted by the master device is associated the transmission indicator transmit the information frame contained in the memory associated with the address and provide its processing unit with an identifier of the address(Figs. 1-11, col.2, liens 20-65); and having the communication circuit of each device for which the address transmitted by the master device is associated with the reception indicator write into the memory associated with the address of the information frame and provide its processing unit with an identifier of the address(Figs. 1-11, col.9, lines 5-col.10, line34);

Therefore it would have been obvious to one ordinary skill in the art at the time of the invention to modify the teachings of Saito to include having the communication circuit of the device for which the address transmitted by the master device is associated the transmission indicator transmit the information frame contained in the memory associated with the address and provide its processing unit with an identifier of the address; and having the communication circuit of each device for which the address transmitted by the master device is associated with the reception indicator write into the memory associated with the address of the information frame and provide its processing unit with an identifier of the address as taught by Osakabe in order to enable the operation of control protocol.

One ordinary skill in the art would have been motivated to combine the teachings of Saito and Osakabe in order to enable the operation of control protocol.

Saito in view of Osakabe does not explicitly teach each device having a plurality of addresses.

Takeda teaches each device having a plurality of addresses(Fig.4-8).

Therefore it would have been obvious to one ordinary skill in the art at the time of the invention to modify the teachings of Saito in view of Osakabe to include device having a plurality of addresses as taught by Takeda in order to identify and terminate connection to devices.

One ordinary skill in the art would have been motivated to combine the teachings of Saito, Osakabe, and Takeda in order to identify and terminate connection to devices.

As per claim 2, the method of claim 1, wherein the processing units of each of the plurality of devices, except for the processing unit of the master device , can neither read nor modify the plurality addresses and the transmission and/or reception indicators of the communication circuit to which they are connected(Saito, para.0058-0059).

As per claim 3, the method of claim 1, wherein all communication circuits further comprise a first address identical for all devices and associated with a transmission indicator and a second address identical for all devices and associated with a reception indicator, the connection of a new device to the network (Saito, para.0058-0063)comprising the steps of: having the master device periodically transmit the first address(Saito, para.0058-0069); having the communication circuit of the new device, upon reception of the first address, transmit an identification frame(Saito, para.0065); having the master device successively transmit the second address and a parameterizing frame defined based on the identification frame(Saito, 0068-0071);

having the communication circuit of the new device, upon successive reception of the second address and of the parameterizing frame, modify its addresses and reception and/or transmission indicators based on the parameterizing frame(Saito, 0068-0071).

As per claim 4, the method of claim 3, wherein each device of the plurality of devices comprises a specific identification number stored in the communication circuit of the device, the identification frame transmitted by the communication circuit of the new device comprising the specific identification number of said new device, the parameterizing frame transmitted by the master device comprising the specific identification number of the new device(Saito, para.0058-0060).

As per claim 5, the method of claim 3, wherein the communication circuit of the new device transmits no data as long as it has not received the first address(Saito, para.0048-0050).

As per claim 6, the method of claim 3, wherein the communication circuit of each device comprises a privilege indicator at a first value when the device is capable of transmitting addresses over the network and at a second value otherwise, said privilege indicator being set to the first or to the second value by the communication circuit of the new device based(Osakabe, Fig.1-11). Motivation to combine set forth in claim 1.

Claims 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Publication 2002/0169886 issued to Saito et al.(Saito) in view of US Patent 5,666,363 issued to Osakabe et al.(Osakabe) in further view of "Memory data register"/"Memory address register" by Wikipedia.

As per claim 7, Saito teaches a device that can be connected to a network comprising: a communication circuit connected to a processing unit and including an address table (Fig.2).

Saito does not explicitly teach the direction table comprising one direction indicator per address, said processing unit being capable of reading information frames stored into the registers or writing information frames in the registers, said communication circuit being capable, upon reception of a request received from the network and corresponding to one of said addresses, of transmitting over the network the information frame stored in the register associated with said address in response to the corresponding direction indicator being a first determined type, of writing an information frame received from the network into the register associated with said address in response to the corresponding direction indicator being a second determined type, and of transmitting to said processing unit an identifier of the register associated with said address.

Osakabe teaches the direction table comprising one direction indicator per address, said processing unit being capable of reading information frames stored into the registers or writing information frames in the registers, said communication circuit being capable, upon reception of a request received from the network and corresponding to one of said addresses, of transmitting over the network the information frame stored in the register associated with said address in response to the corresponding direction indicator being a first determined type, of writing an information frame received from the network into the register associated with said address in

response to the corresponding direction indicator being a second determined type, and of transmitting to said processing unit an identifier of the register associated with said address(Figs.1-11, col.9, lines 5- col.10, line 34).

Therefore it would have been obvious to one ordinary skill in the art at the time of the invention to modify the teachings of Saito to the direction table comprising one direction indicator per address, said processing unit being capable of reading information frames stored into the registers or writing information frames in the registers, said communication circuit being capable, upon reception of a request received from the network and corresponding to one of said addresses, of transmitting over the network the information frame stored in the register associated with said address in response to the corresponding direction indicator being a first determined type, of writing an information frame received from the network into the register associated with said address in response to the corresponding direction indicator being a second determined type, and of transmitting to said processing unit an identifier of the register associated with said address as taught by Osakabe in order to enable the operation of control protocol.

One ordinary skill in the art would have been motivated to combine the teachings of Saito and Osakabe in order to enable the operation of control protocol.

Saito in view of Osakabe does not explicitly teach a register table, and each register in the register table being associated with an address in the address table.

"Memory data register"/"Memory address register" by Wikipedia teaches that memory address register is use to hold the address of the next memory location where

the next instruction is to be executed. Memory data register is a control unit that contains data to be stored in the computer storage or fetch for use.

Therefore it would have been obvious to one ordinary skill in the art to modify the teachings of Saito in view of Osakabe to include using registers as taught by "Memory data register"/"Memory address register" by Wikipedia in order to store information.

One ordinary skill in the art would have been motivated to combine the teachings of Saito, Osakabe, and "Memory data register"/"Memory address register" by Wikipedia in order to store information.

As per claim 8, the device of claim 7, wherein the address table comprises a first address identical for all the devices connected to the network, the direction table comprising a direction indicator associated with said first address of the first determined type, the communication circuit of the device being adapted to transmitting said addresses and the associated direction indicators over the network upon reception of said first address(Saito, para.0017, Osakabe, Figs.1-11, col.9, lines 5- col.10, line 34). Motivation to combine set forth in claim 7.

As per claim 9, the device of claim 8, wherein the address table comprises a second address identical for all device connected to the network , the direction table comprising a direction indicator associated with said second address of the second type, and being capable, upon successive reception of said second address and of a parameterizing frame, of modifying said addresses and the associated direction indicators based on the parameterizing frame(Saito, para.0017,0058-0081, Osakabe, Figs.1-11, col.9, lines 5- col.10, line 34). Motivation to combine set forth in claim 7.

Response to Arguments

Applicant's arguments with respect to claims 1-9 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Examiner's Note: Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in its entirety as potentially teaching of all or part of the claimed invention.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Backhean Tiv whose telephone number is (571) 272-5654. The examiner can normally be reached on M-F 6:30-3:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Follansbee can be reached on (571) 272-3964. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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